CLAIMS

1. A processing device, comprising:

a plurality of processor cores on a common integrated circuit chip, each processor core containing a respective shareable functional unit for performing operations of a first type; and

control logic detecting a failure of a first of said shareable functional units in a first processor core of said plurality of processor cores, and responsive to detecting said failure, placing a second functional unit is a second processor core of said plurality of processor cores in a shared mode of operation, wherein said second functional unit executes operations of said first type originating in said first processor core concurrently with executing operations of said first type originating in said second processor core.

2. The processing device of claim 1, wherein said shareable function units are floating point units for performing floating point operations.

3. The processing device of claim 1, wherein said second function unit comprises:

a set of primary input registers for holding input data to said second functional unit from said second processor core; and

a set of alternate input registers for holding input data to said second functional unit from said first processor core when said second functional unit is in said shared mode of operation.

4. The processor of claim 1, wherein said processing device contains two processor cores.

5. The processing device of claim 1, wherein said shared mode of operation comprises sharing said second functional unit of a cycle-interleaved basis.

6. The processing device of claim 5, wherein said shareable functional units are pipelines, ane wherein said shared mode of operation comprises initiating an operation in said second functional unit from different respective processor cores on a cycle-interleaved basis.

7. The processing device of claim 1, wherein said control logic further detects a failure of said second shareable functional unit, and responsive to detecting said failure of said second shareable functional unit, places said first functional unit in a shared mode of operation, wherein said first functional unit executes operations of said first type originating in said second processor core concurrently with executing operations of said first type originating in said first processor core.

8. The processing device of claim 7, wherein said first function unit comprises:

a set of primary input registers for holding input data to said first functional unit from said first processor core; and

a set of alternate input registers for holding input data to said first functional unit from said second processor core when said first functional unit is in said shared mode of operation.

9. The processing device of claim 1, wherein said first and second processing cores comprise respective functional unit operation queues, each queue holding a plurality of operations for execution by a shareable functional unit.

10. The processing device of claim 1, wherein each said processor core supports the concurrent execution of a plurality of threads.

11. The processing device of claim 1, wherein, if said control logic detects a failure in neither said first functional unit nor said second functional unit, both said first functional unit and said second functional unit operate in a normal mode of operation, wherein said first functional unit executes operations of said first type originating only in said first processor core, and said second functional unit executes operations of said first type originating only in said second processor core.

12. A digital data processing system, comprising:

a memory;

at least one multiple-processor-core device, each said-multiple-processor core device comprising:

(a) a plurality of processor cores on a common integrated circuit chip, each processor core executing at least one respective thread of instructions stored in said memory, each processor core containing a respective shareable functional unit for performing operations of a first type; and

(b) control logic detecting a failure of a first of said shareable functional units in a first processor core of said plurality of processor cores, and responsive to detecting said failure, placing a second functional unit is a second processor core of said plurality of processor cores in a shared mode of operation, wherein said second functional unit executes operations of said first type originating in said first processor core concurrently with executing operations of said first type originating in said second processor core; and

at least one communications bus transmitting data between said memory and said at least one multiple-processor-core device.

13. The digital data processing system of claim 12, wherein said digital data processing system comprises a plurality of said multiple-processor-core devices.

14. The digital data processing system of claim 12, wherein said shared mode of operation comprises sharing said second functional unit of a cycle-interleaved basis.

15. The digital data processing system of claim 12, wherein said control logic further detects a failure of said second shareable functional unit, and responsive to detecting said failure of said second shareable functional unit, places said first functional unit in a shared mode of operation, wherein said first functional unit executes operations of said first type originating in said second processor core concurrently with executing operations of said first type originating in said first processor core.